Abstracts

Low-voltage low-power CMOS-RF transceiver design

M.S.J. Steyaert, B. De Muer, P. Leroux, M. Borremans and K. Mertens. "Low-voltage low-power CMOS-RF transceiver design." 2002 Transactions on Microwave Theory and Techniques 50.1 (Jan. 2002, Part II [T-MTT] (Special Issue on Silicon-Based RF and Microwave Integrated Circuits)): 281-287.

Research over the last ten years has resulted in attempts toward single-chip CMOS RF circuits for Bluetooth, global positioning system, digital enhanced cordless telecommunications and cellular applications. An overview of the use of CMOS for low-cost integration of a high-end cellular RF transceiver front-end is presented. Some fundamental pitfalls and limitations of RF CMOS are discussed. To circumvent these obstacles, the choice of transceiver architecture, circuit topology design, and systematic optimization of the different transceiver blocks is necessary. Moreover, optimization of the transceiver as one single block by minimizing the number of power-hungry interface circuits is emphasized. As examples, a fully integrated cellular transceiver front-end, a low-power extremely low noise-figure low-noise amplifier, and a very efficient power amplifier are demonstrated.

❑ Return to main document.